

VLSI Design 6332

Design Review 1

A Method to Implement Low Energy
Read Operations, and Single Cycle
Write After Read in Subthreshold
SRAMs

by

The Sub-threshold Team
Author
Arijit Banerjee

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Chapter 1

Summaries of Papers

In [1], the authors proposed a novel 10T differential SRAM bitcell which is based on Schmitt Trigger (ST). They claim to have achieved 1.56X higher read static noise margin(RSNM) at the supply voltage of 400 mV compared to the conventional 6T bitcell. As the ST bit cell is of differential type incorporating the same within a 6T bitcell based SRAM does not require architectural changes. They also claim that with iso-area and iso-read failure probability the novel ST bit-cell operates at supply voltage of 175mV with 18% reduction in leakage and 50% reduction in read and write power compared to the conventional 6T bitcell. They showed simulation data of the ST bitcell having data retention voltage as low as 150mV.

In [2], the authors proposed a differential 10T bitcell which separates the read and write operation effectively and reportedly to be achieved higher cell stability. The bitcell also provides superior bit-interleaving structures to achieve soft-error tolerance with conventional Error Correcting Codes (ECC). They claimed to be had incorporated DCVSL scheme to compensate bitline leakage with improved bitline swing. They verified their bitcell by fabricating 32KB array of the 10T bitcell in 90nm CMOS technology which claimed to be operational at 160mV.

In [3], the authors proposed various circuit techniques for designing robust high-density sub-threshold SRAMs. Their methods includes improving read margin by decoupled cells, utilizing the reverse short channel effect RSCE to improve write margin, eliminating data dependent bitline leakage to enable longer bitlines, virtual ground replica scheme for the improvement of bitline sensing margin, write back scheme for preservation of data during write, and using sub-threshold logical effort to size gates optimally.

In [4], the authors examined the impact of process variation for low voltage operations in 65nm sub-threshold SRAMs. They compare various bitcells' pros and cons and introduce a 10T bitcell with 4T read buffer for improved leakage. The usage of M10 in the bit cell drops the leakage overhead to 16% than that of a 9T cell compare to a 6T bitcell with iso-VDD. They reported that the 10T at 300mV consumes 2.25X less leakage than that of the 6T bitcell operating at 0.6V. This SRAM functions below 400mV. At 400mV the power consumption is 3.28uW with working frequency of 475KHz maximum. They also reported that the leakage power being reduced by VDD scaling was 2.4X and 3.8X relative to 0.6V operation at 0.4V and 0.3V respectively.

In [5], the authors proposed a 9T SRAM bitcell for low voltage and energy constrained applications. They claims that the 9T bitcell at 32nm PTM technology node shows 37% improvement in the read stability compared to 6T bitcell at 0.9V. The standard deviation of Read SNM (RSNM) for the

proposed bitcell is claimed to be 54% lesser than that of the 6T at 0.9V. They also claimed that at the supply voltage of 400mV the mean of the RSNM is 23% higher than that of the standard 6T bitcell. The proposed design allows to optimize RSNM and WSNM, and writing speed separately avoiding the conflicting sizing in the 6T scenario.

In [6], the authors proposed a read-assist circuit in 65nm CMOS technology which reduces the access time significantly and improves the SRAM cell stability. In this circuitry they used a set of per-amplifiers in bit-lines to amplify the swing ahead of time to evaluate earlier with 3x reduction of bitline actual swing. They compared there proposed scheme to conventional circuitry and other state of art design which showed a speed improvement of 53% and power reduction of 21.3%. They also claimed that the proposed scheme enabled them to reduce the cell supply voltage by 227mV to operate at 560mV with the same evaluation time of 700 ps.

Chapter 2

Printout of Simulation Results and Corresponding Schematics

Observations from the Papers:

In [1], from the Fig. 8 (a) of the [1] shows that the Monte Carlo (MC) data indicating “mean-3sigma” RSNM of ST is lying in between 50mV to 0mV and “mean – 3sigma” hold signal to noise margin (HSNM) lying nearby 100mV. On the other hand in Fig. 9 the “mean + 3sigma” V_{min} looks like lying in between 350-400mV. Hence, from the process variation and robustness standpoint with 400mV of supply voltage the 3sigma worse case values indicates that there may be failures in the bitcell in below 350mV if fabricated.

In [2], from the Fig. 7 it can be seen that the 3sigma worst case Read and Hold SNM is not robust at all. With 300 mV supply the “mean – 3sigma” WSNM is around 100mV, and “mean + 3sigma” Hold SNM is about 85mV, and “mean – 3sigma” read SNM becomes negative.

In [5], the Fig. 6, 7, 8 and 9 shows RSNM distributions of the proposed bitcell versus standard 6T bitcell. It can be referred from the plots that at 400mV the worst case “mean – 3Sigma” RSNM is around 20mV, and due to this fact there can be read failures from the standpoint of process variation.

Our findings from studying the papers is that below 400mV most of the published SRAM bitcells are having issues with robustness standpoint limited by the bitcells’ worse case RSNM, VDRV, RSNM, HSNM, V_{MIN} perspective which may lead to failures if the supply voltage is lowered further in subthreshold domain. Hence, lowering dynamic energy consumption in SRAM by lowering supply voltage is been hindered by the poor robustness in below 400mV supply voltage in SRAM bitcells. Hence, we try to research other ways to mitigate energy consumption in sub-threshold SRAMs. The method mentioned in [3] as writeback is a common way to avoid the half select problem in subthreshold SRAMs. We propose a method to utilize the concept of writeback to implement low energy read operations. In our Method we implement 128bit intermediate latches in the global bitlines to latch all the 8 words (16 bits) in a normal write after read (writeback), and read operation, and if the user reads from the same row in two or more consecutive read operation the Read Word Line (RWL) does not toggle and we just read from the intermediate latch. With this scheme we save a lot of dynamic energy by not switching RWL and row decoders. Hence, we should be consuming much less power in consecutive read operations in which operating components of the memory are 16 bit output flip-flop, 128 to 16 bit bus interface logic, and input flip-flops.

Motivation:

There was a version of sub-threshold data memory used in UVa Body Sensor Network (BSN) chip last year. The memory had normal 128 bits of DIN and DOUTs directly providing to the user with operating

voltage of 0.5 volt and frequency of 200 kHz. In the memory the writing operation was done in effective two cycles by write after read approach which is standard in sub-threshold memories to avoid the half select issue. Recently the BSN chip team has changed the ISA along with the bus width of the main data and address bus to 16 bit each, and they demanded new features in the memory like somehow single cycle effectively writing, lowering the read dynamic power dissipation, and other features like including input and output flops, converting the existing 128bit bus to 16 bit bus interface to the SOC, and so on. In order to meet their requirements we added new circuits and modified the Data memory to meet the specification.

Annotated full schematic of 4KB subthreshold SRAM data memory:

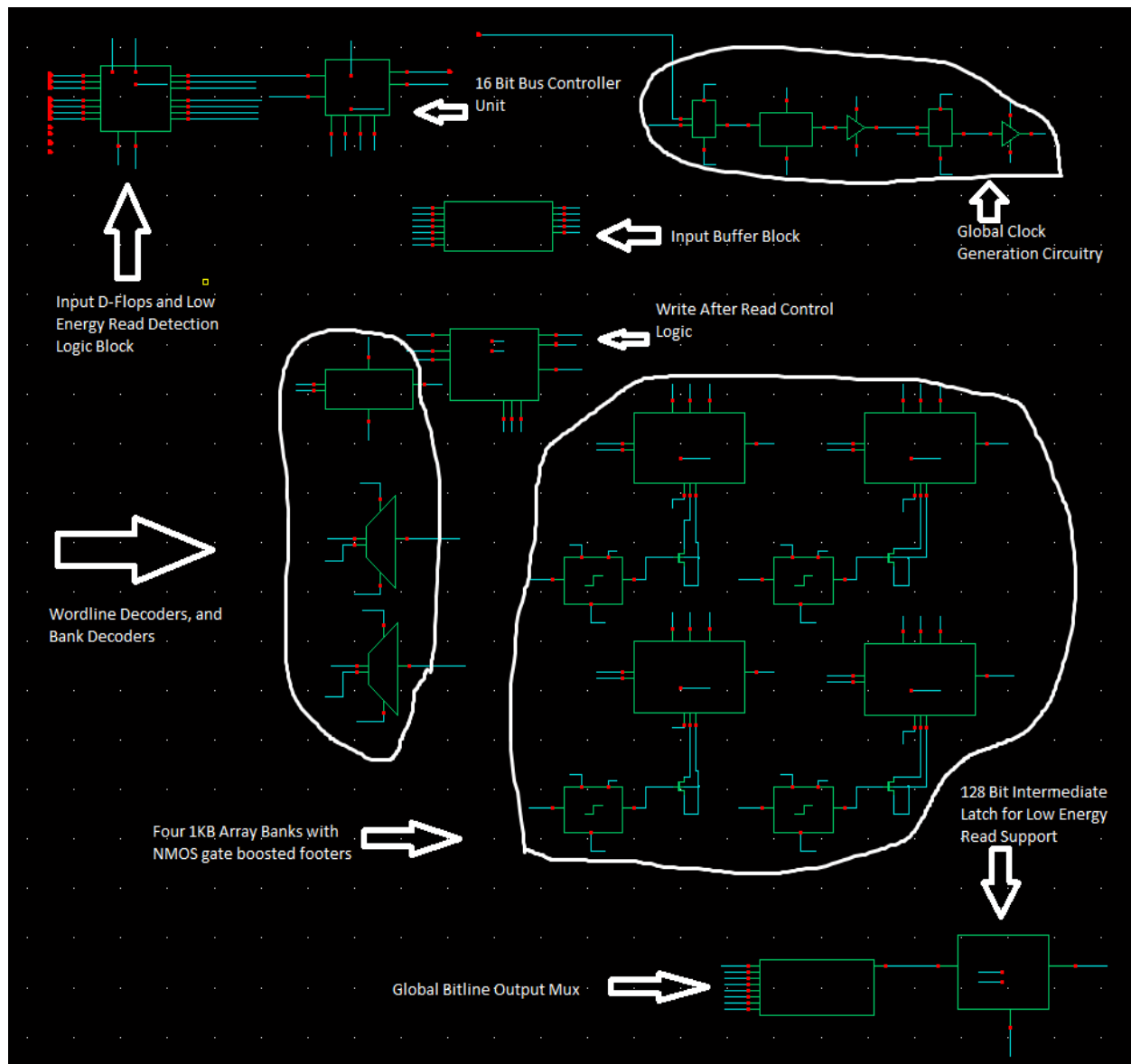


Fig. 1-a

Simulated and annotated waveform of the single cycle write after read, and normal read operations:

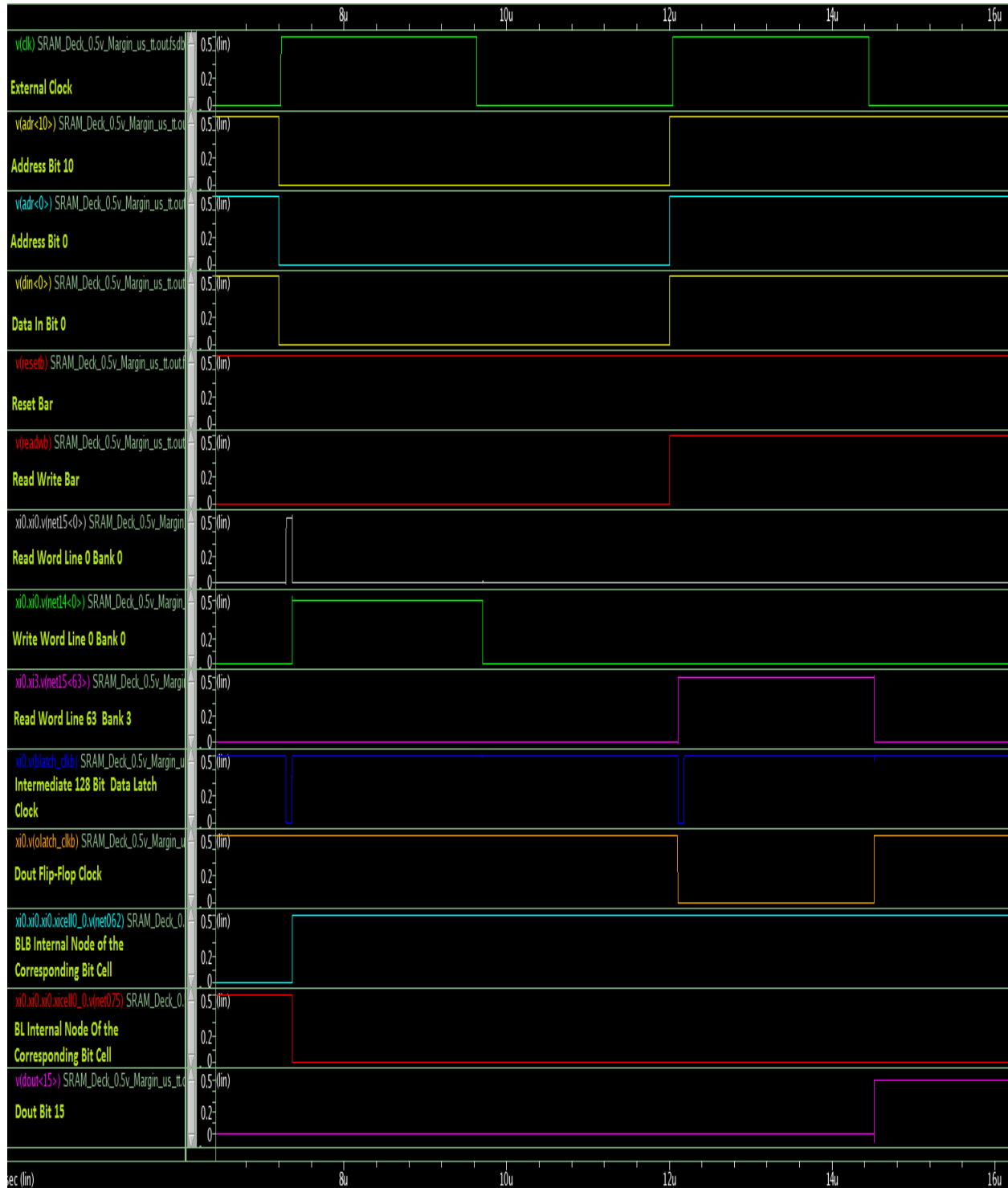


Fig. 1-b

Simulated and annotated waveform of the low energy read operations:

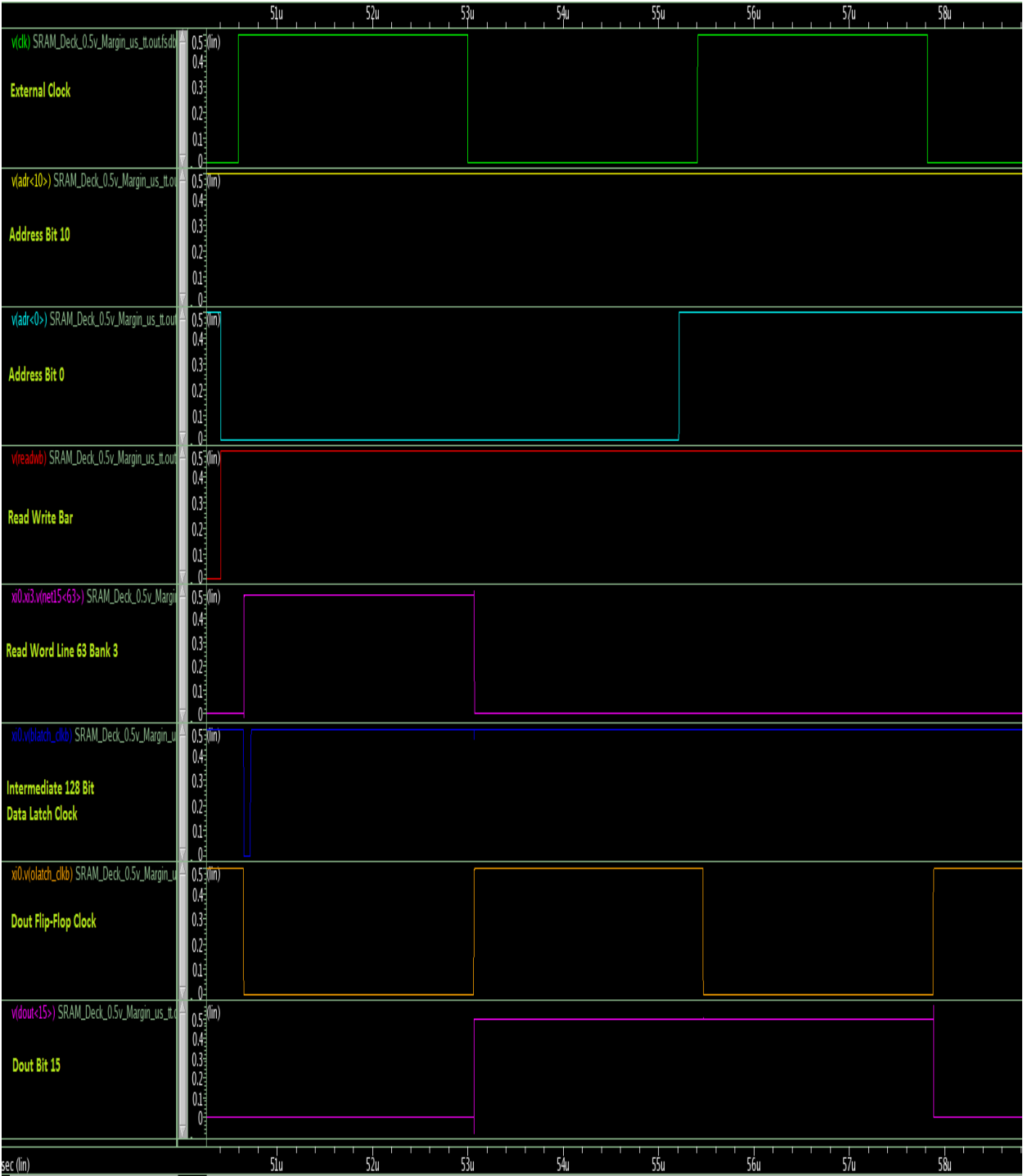


Fig. 1-c

Annotated schematic for low energy read operation support in 4KB subthreshold SRAM data memory :

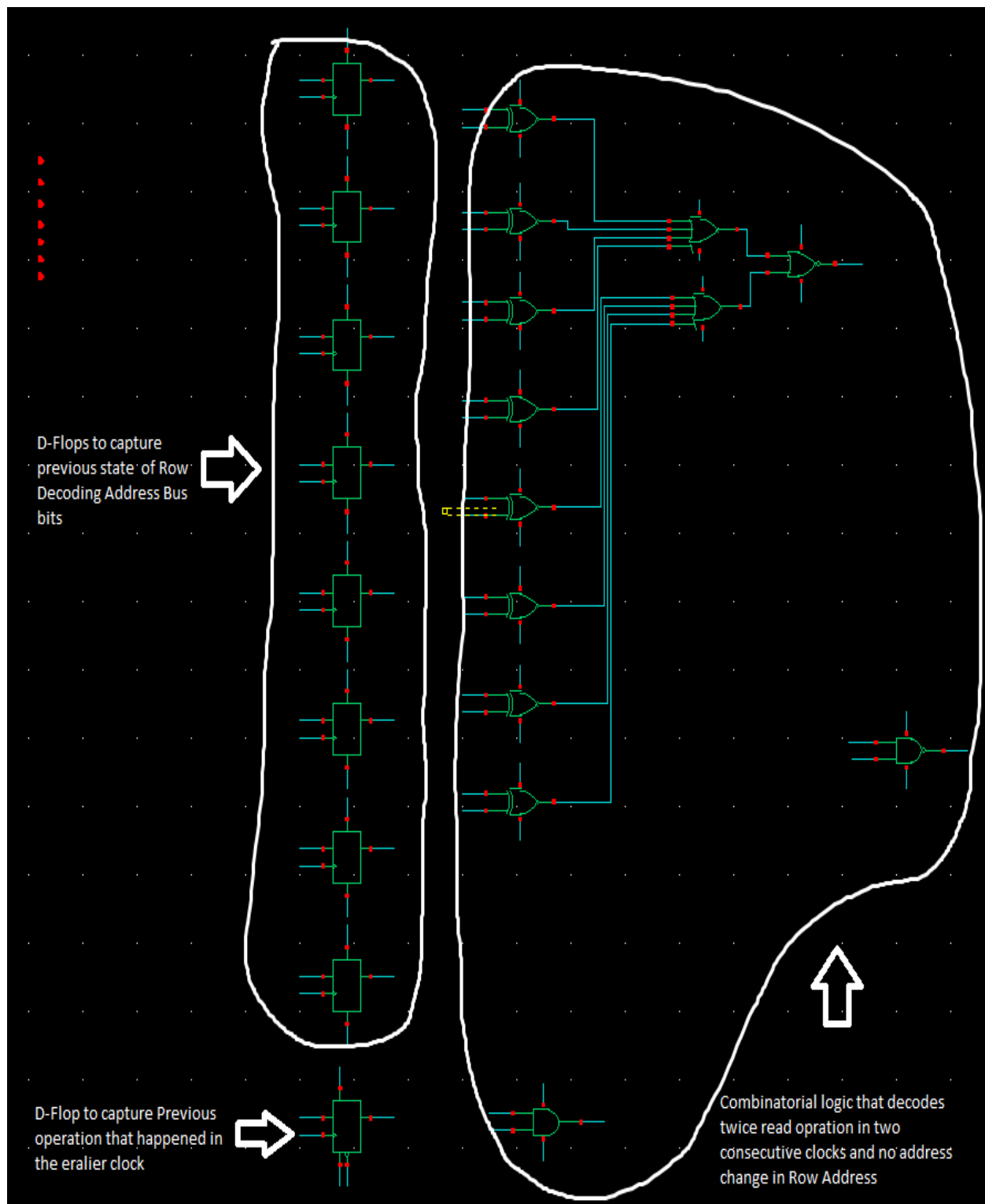


Fig. 2

Annotated schematic for single cycle write after read control logic, output-flop, and 128 bit intermediate latch clock generation logic in 4KB subthreshold SRAM data memory :

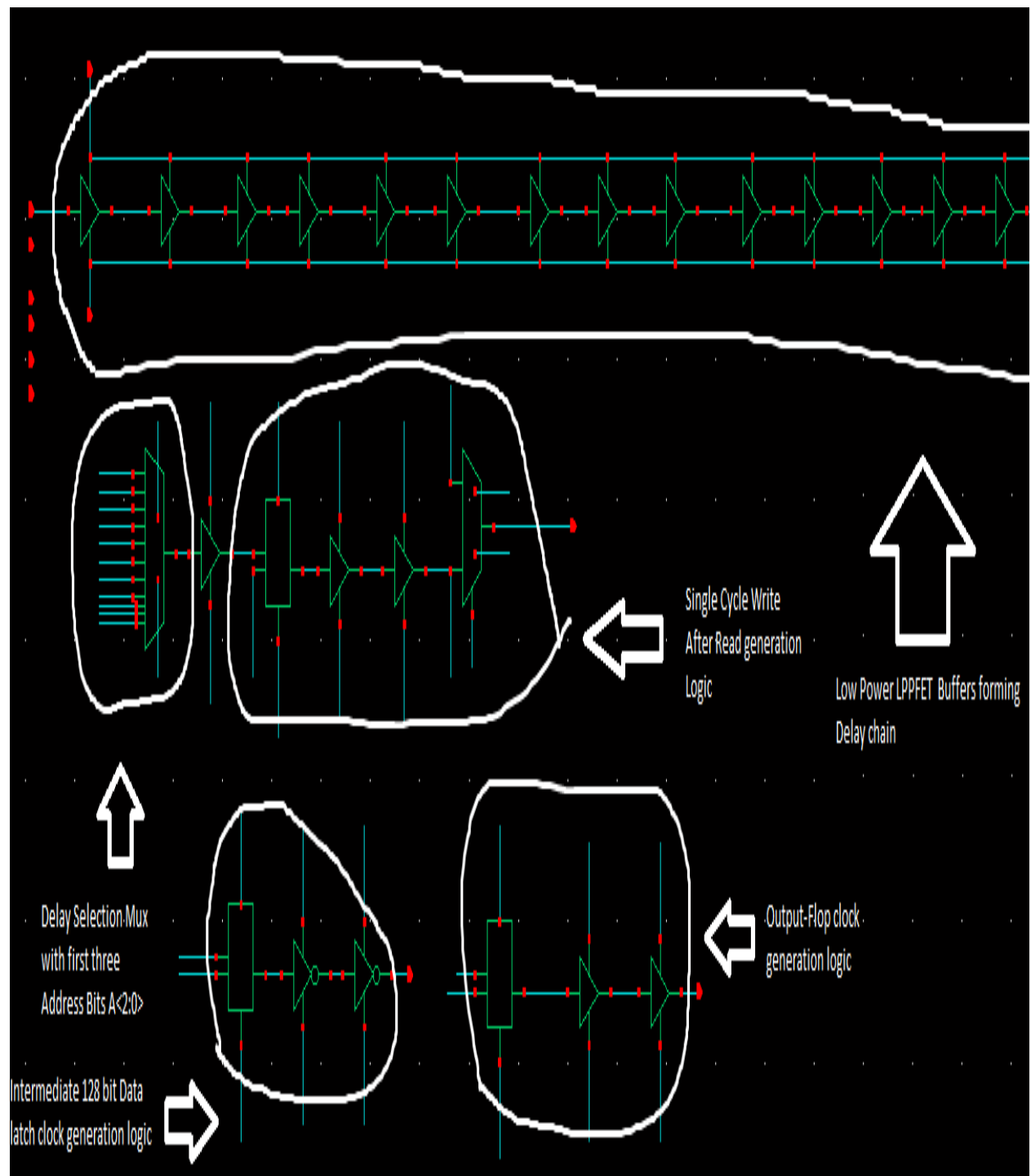


Fig. 3

16 bit bus controller and 128-to-16bit bus interface logic:

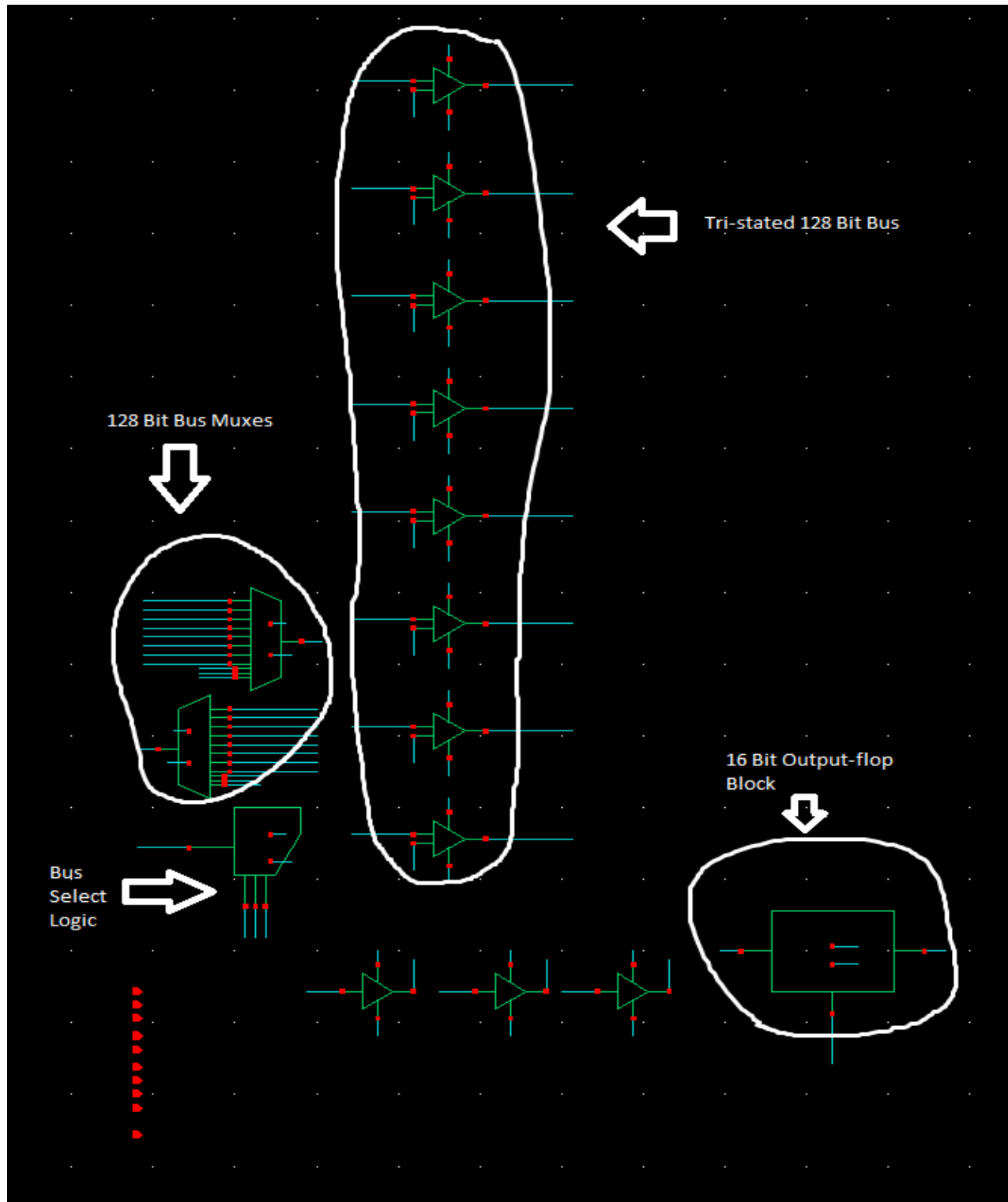


Fig. 4

Chapter 3

Report on our Group's progress

Progress:

We already build these above sub-circuitry for low energy read operation support, single cycle write after read, 128 to 16 bit bus multiplexers, intermediate 128 bit latches and input and output flops. As this memory will always be operated at room temperature, we are simulating the same in 27C temperature only. We have simulated our sub-threshold memory in PVT of TT_0.5V_27C corner and the functionality we are getting from simulation is what we intended. The supply voltage of 0.5V was chosen by the BSN chip group as the supply for the digital logic used is 0.5v. The memory is already been working with the supply voltage near by the “mean +3 sigma” DRV Vmin of the bitcell which is nearly 350mV.

We distinctly separate tasks prior to the proposal, and following the proposal as follow:

Tasks prior to the proposal:

- i) Simulation and debugging for functionality of the 4KB Data Memory in all process corners
 - a) TT, FF, SS, SF and FS
 - b) With all WR modes starting from WR<0:3>=000 to WR<0:3>=111
 - c) Measurement of the Energy Savings in Low Energy Mode for TT corner

Remaining Tasks following the proposal:

- ii) Measuring the Energy Saving in Low Energy Mode for in TT, FF, SS, SF and FS corners
- iii) Checking Design Margins in TT, FF, SS, SF and FS for at least one WR mode
- iv) Building Layouts of each new component block
- v) Integrating Layouts to Data Memory
- vi) Running DRC and LVS
- vii) Extracting Lumped parasitics
- viii) Simulate in TT corner with lumped parasitics
- ix) Further simulate FF, and SS corner with lumped parasitics
- x) Sign off and Tape out on November 6th 2012

Chapter 4

References

- [1] J. P. Kulkarni, K. Kim, and K. Roy, "A 160 mV Robust Schmitt Trigger Based Subthreshold SRAM," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 10, pp. 2303–2313, Oct. 2007.
- [2] I. J. Chang, J.-J. Kim, S. P. Park, and K. Roy, "A 32 kb 10T Sub-Threshold SRAM Array With Bit-Interleaving and Differential Read Scheme in 90 nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 2, pp. 650–658, Feb. 2009.
- [3] T. H. Kim, J. Liu, J. Keane, and C. H. Kim, "A high-density subthreshold SRAM with data-independent bitline leakage and virtual ground replica scheme," in *Solid-State Circuits Conference, 2007. ISSCC 2007. Digest of Technical Papers. IEEE International*, 2007, pp. 330–606.
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- [5] G. K. Reddy, K. Jainwal, J. Singh, and S. P. Mohanty, "Process variation tolerant 9T SRAM bitcell design," in *Quality Electronic Design (ISQED), 2012 13th International Symposium on*, 2012, pp. 493–497.
- [6] Ali Valaee, Asim J. Al-Khalili, "SRAM Read-Assist Scheme for High Performance Low Power Applications" in *International SoC Design Conference (ISOCC), 2011*, pp. 179-182.